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Reduction of Current Leakage in VLSI Systems

[1]Tayab Mustaq Ahmed [2] Deepak H.A
[1]3rd year,
[2]Professor
[1][2]Electronics and Communication Department, NDRK Institute of Technology, Hassan-573201.

***Abstract**: This paper consisting of the general information about the VLSI followed by the history and development of the VLSI. MOORE's LAW is explained shortly and the designing of the VLSI circuits is explained by the design of VLSI by HIERARCHY-STRUCTURE. In this paper some of the general discussion on the current leakage reduction in the processors are discussed in which the reduction of current leakage by using switches are included and also we can reduce the current leakage in the circuit by using "sleep transistor". Sleep transistors are the transistor which turns off completely when the circuit is not in use. This is a very effective technique. After that some of the discussions about the problems in implementing the sleep transistors is also discussed which is very important while designing any circuit.*

I. Introduction

Very Large Scale Integration

Very large integration (VLSI) is the process of creating an integrated circuit(IC) by combining thousands of transistors into a single chip.VLSI is basically originated and began in year 1970's.At that time the complex semiconductor and communication technology were being developed. One of the example for VLSI device is microprocessor.Before implementing VLSI technology most of the IC's had a limited set of function they could perform and consist of limited set of hardware. An electronic circuit at that time consist of CPU,ROM,RAM, and other logic components. But by implementing VLSI technology IC designed were consist of all the above component in a single chip.The electronic industry has achieved a phenomenal growth over the last few decades, mainly due to the rapid advances in large scale integration technology and system design application with the advert of Very large scale integration(VLSI) design the number of applications of IC's in Higher-performance computing controls, telecommunication, image and video processing and consumer electronics has been rising very fast. Due to the advancement of the technology and the vast use of IC's in cellular communication and other hardware purposes the trend of VLSI design is expected to grow rapidly every year.

II. History

During the mid-1920's several inventors attempted devices that were intended to control current in solid state diodes and convert them into triodes. But the success did not come until word war II, during which the attempt to improve silicon and germanium for the use in the radar detectors led to the improvement in the fabrication and in the understanding the quantum mechanical states of carriers in semiconductor. Then scientists who had been diverted to radar development returned to solid state device development with the invention of transistor at Bell Labs in 1947, the field of electronics shifted from vaccum tubes to solid state devices.At the time the electrical engineers of 1950's saw the possibilities of constructing far more advanced circuits than just transistors, as the complexity of the circuit grew the problems were arised one of the greatest problem at that time was the size of the circuit. A complex circuit like a computer was dependent on speed. If the components of the computer were too long the time required for the electricity to flow will be less and this device could not be effective to use. Then in 1958 Jack Kilby at Texas instruments found a solution for that problem his idea was to make all the component of the chip out of the same block(monolith) of semiconductor material. Kilby presented this idea to his superiors and got permission to built his first IC in 1958. Although the 1st IC was crude and had some problems but the idea was mind blowing. Bymaking all parts of the chip by using same material, the use of extra wires is reduced and no discrete components are required and the circuit could be made smaller and the manufacturing process could be automated.From here the idea of integrating all components on a single silicon wafer came into existance , which led to the development in small scale integration(SSI) in 1960's, then came medium scale integration(MSI) also in 1960's after that in 1970's and 1980's came the large scale integration(LSI) and very large scale integration (VLSI) with tens of thousands of transistors on a single chip is raised to hundreds of thousands and now it has reached to billions of transistors in a single chip.

III. Development

The first semiconductor chips had two transistors each of them but after time more and more transistors were added and more systems were integrated over time. The first integrated circuit had only a few devices, perhaps as many as ten diodes, transistors, resistors and capacitors making possible to fabricate only one or more logic gates on a single device, now which is known as small scale integration(SSI). Then they implemented atleast hundreds of logic gates in a single device this process is known as medium scale integration(MSI).Then they implemented atleast thousands of logic gates and this is known as the large scale integration(LSI).Now a days current technologies consists of millions of gates integrated in it and this is called as the very large scale integration(VLSI) and the implementation of logic gates beyond this number is known as Ultra-large scale integration(ULSI).The term suggesting greater than VLSI is not in use anymore.

IV. Moore's Law (4)

Moore's law is the observation that the number of transistors in a dense integrated circuit doubles approximately every two years. The observation is named after Gordon Moore, the co-founderof Intel and Fairchild Semiconductor.

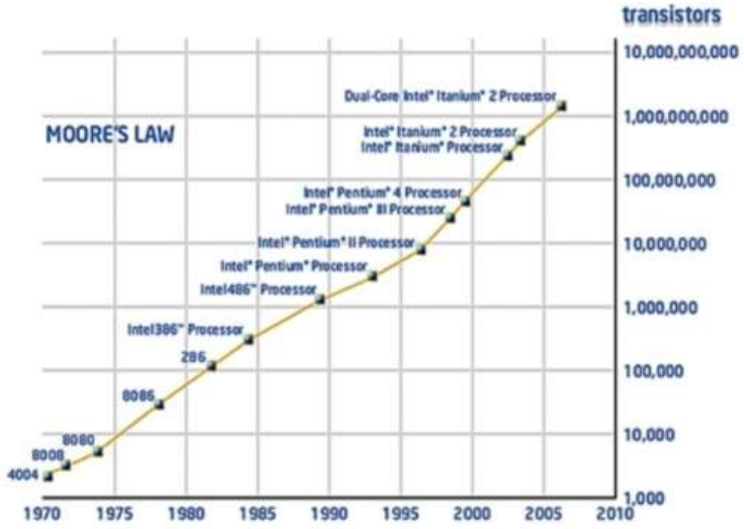


Fig 1.1

The above graph shows how the development of processors took place year by year, as we observe the graph we can see that the transformation of processors which containing hundred or thousand IC is now advanced to be containing millions of IC's in a single chip.

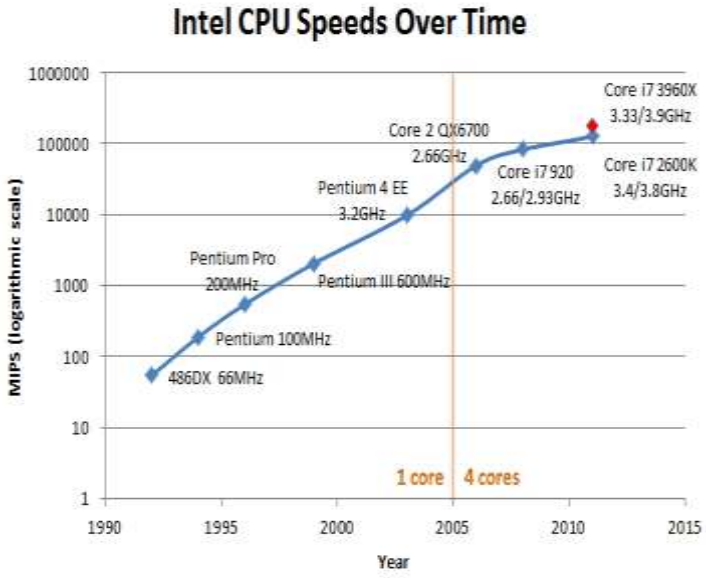


FIG1.2

The graph shows the transformation of speed of the Intel processors from time to time. As the Moore stated that the number of transistor will increases every two years like that only we can see in the development of the INTEL processors from time to time how the processors are developed from C-4004 to INTEL i7 core processor. We were able to increase the number of transistors used in the chip, from around 100 transistors to billons of transistors in a single chip. And we also have increase the speed of the processors.

V. Design

Designing of the circuit is one of the important and basic step while making a processor. Designing a circuit as that the manufacturing shall be easy and the complications in the circuit should be lesser is very important. In the below topic we have discussed some things about the designing of a structure using Hierarchy principle. In which 16-bit adder circuit is divided into half adder. As we know that the construction of Half adder is very easy when compared to the 4-bit adder. And the output obtained in the circuit is same and is not affected by the change in the circuit.

Design of Hierarchy-Structure

The design hierarchy involves the principle of "Divide and Conquer". It is nothing but dividing the task into smaller task until it reaches to its simplest level. This method is very much suitable because the last evolution of the design has become so simple that its manufacturing becomes easier. Let's take an example of 16-bit adder, Here the 16-bit adder is divided into four modules of 4-bit adder. Then each 4-bit adder is divided into module of 1-bit adder or Half adder which easy to fabricate and simplest to design process. Its internal circuit is also easy to fabricate on the chip. Now by adding the last four adders we can design a 4-bitadder and moving on we can design a 16-bit adder.

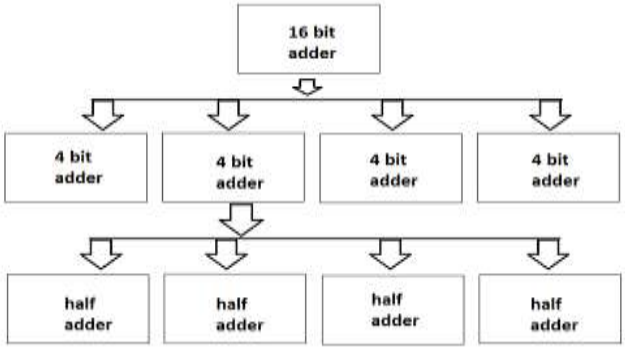


FIG 1.3

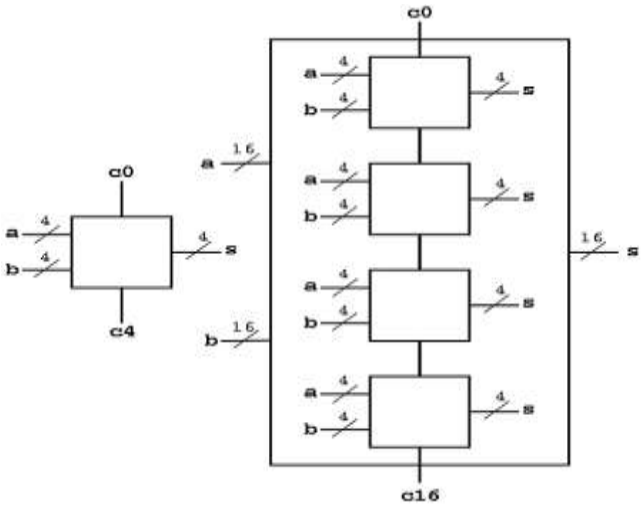


FIG 1.4

In the above 2 figures we can see how a 16-bit adder is divide into 1-bit adder and the output obtained is 16-bit. The output obtained is same but the method of dividing made the circuit simpler to design.

VI. Y Chart

The Gajski-Kunn Y-chart is a model, which captures the consideration in designing semiconductor devices. The three domains of Y-chart are on radial axes. Each of domains can be divided into levels of abstraction, using concentric rings. AT the top level or the outer ring, we consider the architecture of the chip, at the lower level or the inner rings we successive refine the design into the fines de tailed implementation. Creating a structural description from a behavioral one is achieved through the process of high-level synthesis or logical synthesis. Creating a physical description from a structural one is achieved through layout synthesis.

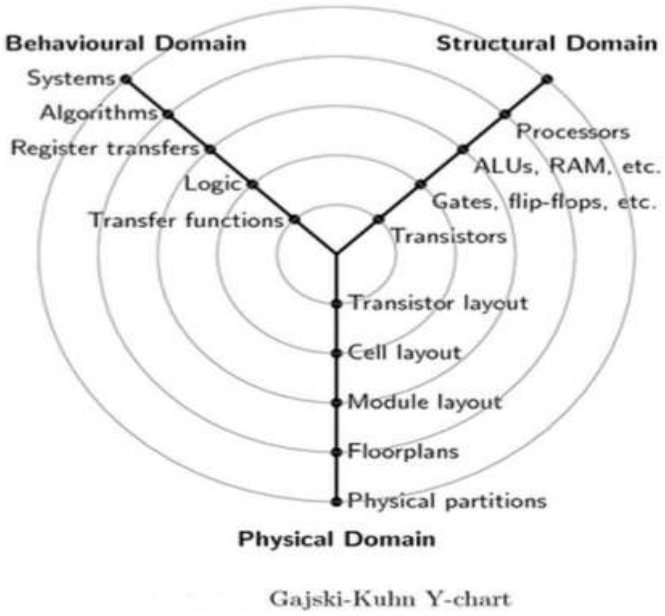


FIG 1.5

VII. Leakage Current Reduction Technique

A) Leakage of Current

Leakage of current is one of the major problem when designing a low power VLSI device, and is getting more and more as the technology is developing. In the older technology the consumption of more power is not important but when we go deep into sub-micro technology the higher static power consumption due to the leakage of current becomes a critical issue. MOSFET threshold voltage is one of the key point in low power VLSI design. One should consider carefully whether the circuit they design operates below threshold voltage or above threshold frequency. We want a differential amplifier topology to operates in low power and hence we can use power gating i.e., applying the controlled switches at the head or tail of the transistor. An adding of a switch for lower power consumption may yield us load device to operate at under the threshold voltage. Although this technique is not exactly suitable in this case but it possible to reduce the leakage of current by this process.

B) Managing the Leakage of Current by Using Sleep Transistors

As the geometry of the transistor get smaller the leakage components, including both sub threshold and gate leakage have become a bigger problems. The leakage of power can take up on a significant portion of the overall chip power but, this can be controlled by using one of the efficient and relevant technique i.e., using of SLEEP TRANSISTORS using sleep transistors can reduce the transistor current leakage. Applying the sleep transistors in between normal circuit blocks and power supply rails, apply this at either end at v_{ss} or v_{cc} or both. Sleep transistor have a very unique character that it can shut itself off completely when the circuit is not accessed. This blocks the flow of the current and hence the leakage of current can be reduced up to an extent. When the sleep transistors are turned off, the power supplies at vcc and vss across the function block will be collapsed towards the centre, as a result the voltage difference across the transistor gate as well as source and drain is lowered. Which reduces the leakage significantly. The designing of the sleep transistor is simple. In this we need to add the "SLEEP" circuit at both the ends of the circuits i.e., V_{DD} and ground. We can take a simple example of NAND gate implementation. In which the "SLEEP" circuit is installed at the either end of the V_{DD} and ground.

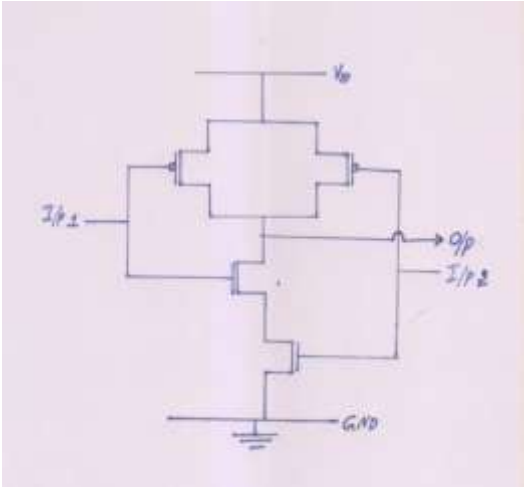


FIG 1.6

NAND Gate

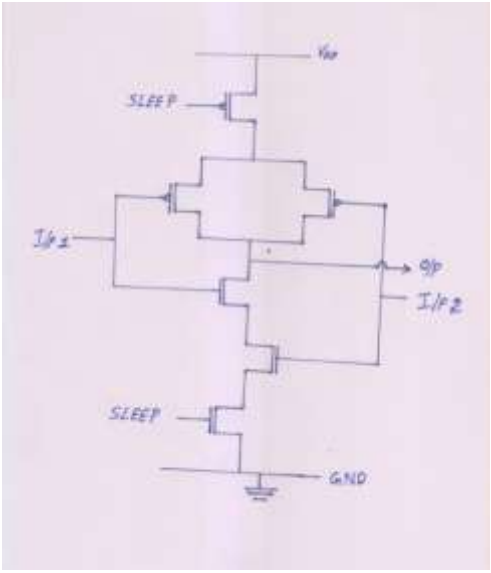


FIG 1.7

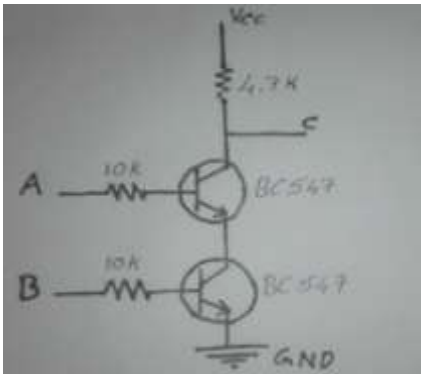
Sleep Approach of NAND Gate

In the above given figures shows is the NAND gate. In fig 1.6 shows the normal NAND gate and fig 1.7 shows the NAND gate development using the sleep approach if we observe in both the figure we can see that the basic core of NAND gate is same only change in the circuit is that fig 1.7 consist of sleep circuit a both the ends i.e., at V_{DD} and ground. In general NAND gate transistor the circuit does not shut down completely when not in use. Even if it is off it consumes small amount of current or the current is wasted. But when we move on to the sleep transistors NAND gate, whenever there is no need of circuit or whenever the circuit is not in use it automatically shut off the whole circuit or block the supply of current in the circuit and hence no extra power is consumed and by this we can control the leakage of current in the processor or transistor. So, we can use the sleep transistor in place of the normal transistors to control the leakage of current in the processor. Using of sleep transistor is one of the best and effective method of controlling the leakage of current and hence can be implemented in the processors. Although to implement the sleep circuit in a normal transistor we need to change the design structure of the transistor, but by changing this we can make a current efficient micro-processor which can be a very bigger level of development in the field of VLSI or the development in the field of hardware technology. By using the sleep transistors it won't also effect the memory capacity of the chip neither the speed of the chip is effected, which is very much essential while designing. This is important because we need to develop a better functional chip by not affecting the present useful features.

VIII. Designing The Circuit Using Simple Method

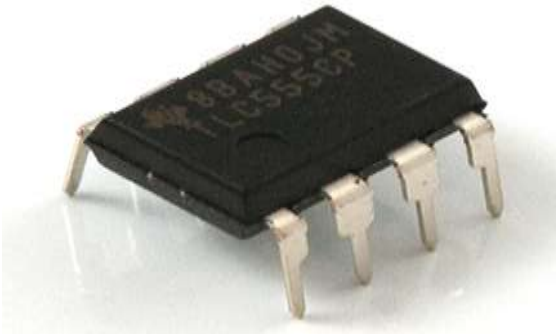
In this part we can study the mechanism using a simple transistor circuits. Which means we study the working of a sleep circuits using 555 Timer IC. It is used only to see how the circuit works. When we switch to the MOSFET transistor it will be hard to understand so, we have explained the whole process using the simple transistors which will be easy to understand the whole process. Hear instead of the sleep transistor we have used the 555 Timer Circuit. In this circuit the timer is set to turn off the circuit after a time interval of 2.25 minutes. These below circuits are used to understand the working purpose only.

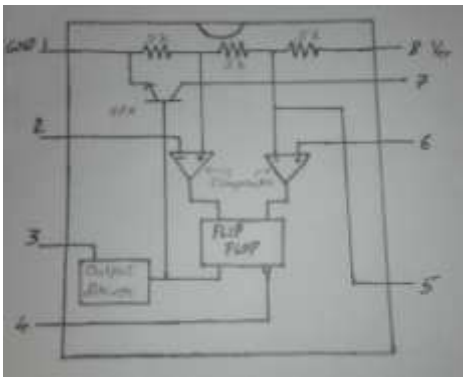
A) **NAND Gate**



The above shown figure shows the basic structure of a NAND gate which is constructed using simple components like transistor and resistors. We have not used any MOSFET transistors, because to keep the circuit simple. In the above figure the point A and B are the inputs and the point C is the output of the overall circuit and the transistor used is BC547.

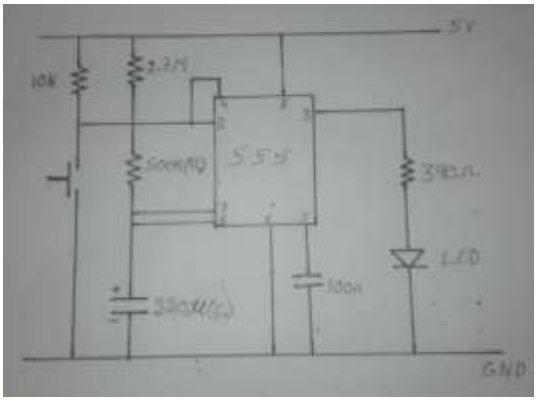
B) **555 Timer IC**





The following above figure shows the internal structure of an 555 IC which can be used as a timer circuit or a sleep circuit. This circuit can be easily combined with any other IC circuits. As we can see in the figure the internal circuit of the 555 IC can be easily implemented in any IC by using limited or lesser space.

C)**Sleep circuit using 555 IC**

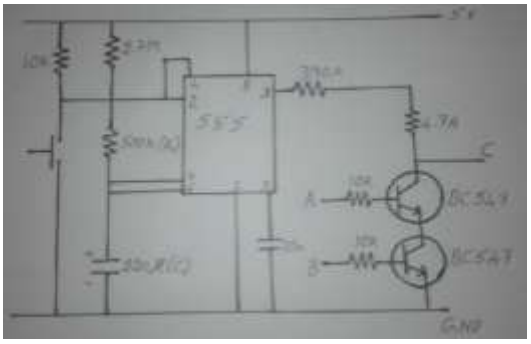


The above shown figure is the sleep circuit which is constructed using 555 timer IC. This above circuit is constructed on the basis of the capacity to turn off automatically after 2.25 minutes. We can also design the circuit for more time interval or lesser time interval of turning off according to our need. We can alter the time interval by varying the value of the capacitor or resistor value at the pin 6 and 7 respectively i.e., by changing value of R_1 and C_1. To set a required time interval the following formula can be used i.e., **$T=1.1*R_1*C_1$**

As per our requirement we have set the timer for the time interval of 2.25 minutes so, we can check the value of the resistor or capacitor as per our need for example

$T=1.1*R_1*C_1$
$T=1.1*(560k)*(220*10^{-6})$
T=135.52sec
T=2.25 minutes

D) **Sleep approach for NAND Gate**



In the above figure it shows the sleep approach of the NAND gate circuit. As we can observe in the above circuit the output of the sleep circuit is connected to the V_{cc} of the NAND gate and the other is connected to the ground. The input A and B of the NAND gate is not changed and also the output C is also not altered. In the above circuit the NAND gate is automatically turned off after the time interval of 2.25 minutes and get ON when the input is changed in the circuit. By this approach we can reduce the current leakage in VLSI system. Because when there is no current is passing through the circuit when its not being used, then the wastage of current is reduced.

IX. Drawbacks Of Using Sleep Transistors

1. It requires modification of CMOS technology to support both high V_T device for sleep transistor and low V_T device for logic gates.
2. It decreases the DC noise margin as it decreases the voltage swing.
3. Decrease in the threshold voltage of the sleep transistor due to the supply voltage scale-down each generation. That mean the leakage of the current will continue to increase exponentially with every generation.
4. Sleep transistor sizing is not a easy task and requires more effort.

X. Conclusion

From this following paper we can conclude that the use of the sleep transistors are very much favourable and can be generally used to reduce the leakage of current or the wastage of current the circuit. Although there are some of the problems while designing or the implementation of the circuits, but this method is most desirable to design a current efficient circuit. And also designing of the IC's with less power consumption is required now a day for the development in the field of hardware technology.

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